FORM PTO-1449

INFORMATION DISCLOSURE STATEMENT

ATTY. DOCKET NO.	APPLICATION NO.
1997.0010003	09/698,249
APPLICANT: Fu *et al.*	
FILING DATE: October 30, 2000	GROUP: 2124

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA1	3,646,337	02/1972	Bifulco, Jr.			
	AB1	3,974,367	08/1976	Mayer			
	AC1	4,340,939	07/1982	Mayer			
	AD1	4,719,833	01/1988	Katoh *et al.*			
	AE1	5,276,633	01/1994	Fox *et al.*			
	AF1	5,373,236	12/1994	Tsui *et al.*			
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EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
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	AK	1	Ahn, Y. *et al.*, "VLSI Design Of A Cordic-Based Derotator," *Proc. 1998 IEEE Int. Symp. Circuits Syst., Vol. II*, pp. 449-452 (May 1998).
	AL	1	Andronico, M. *et al.*, "A New Algorithm for Fast Synchronization in a Burst Mode PSK Demodulator," *Proc. 1995 IEEE Int. Conf. Comm.*, Vol. 3, pp. 1641-1646 (June 1995).
	AM	1	Arivoli, T. *et al.*, "A Sinle Chip DMT Modem for High-Speed WLANs," *Proc. 1998 Custom Integrated Circuits Conf.*, IEEE, pp. 9-11 (May 1998).
	AN	1	Boutin, N., "An Arctangent Type Wideband PM/FM Demodulator With Improved Performance," *IEEE Trans. Consumer Electron.*, Vol. 38, No. 1, pp. 5-9 (February 1992).
	AO	1	Buchanan, K. *et al.*, "IMT-2000: Service Provider's Perspective," *IEEE Personal Communications*, pp. 8-13 (August 1997).
	AP	1	Chen, A. *et al.*, "Modified CORDIC Demodulator Implementation for Digital IF-Sampled Receiver," *Proc. Globecom 1995*, Vol. 2, pp. 1450-1454 (1995).

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	AA2	6,144,712	11/2000	Samueli *et al.*			10/09/1997
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	AK	2	Chen, A. *et al.*, "Reduced Complexity CORDIC Demodulator Implementation for D-AMPS and Digital IF-Sampled Receiver," *Proc. Globecom 1998*, Vol. 3, pp. 1491-1496 (1998).
	AL	2	Cho, K., *A Frequency-Agile Single-Chip QAM Modulator with Beamforming Diversity*, Dissertation Submitted to the University of California, Los Angeles, 137 pages (1999).
	AM	2	Critchlow, D.N., *The Design and Simulation of a Modulatable Direct Digital Synthesizer With Non Iterative Coordinate Transformation and Noise Shaping Filter*, Thesis Submitted to the University of California, San Diego, 55 pages (1989).
	AN	2	Daneshrad, B., Ph.D., *System design of a 1.6 Mbps all-digital QAM transceiver for digital subscriber line applications*, Dissertation Submitted to the University of California, Los Angeles, 156 pages (1993).
	AO	2	Erup, L. *et al.*, "Interpolation in Digital Modems - Part II: Implementation and Performance," *IEEE Transactions on Communications*, Vol. 41, No. 6, pp. 998-1008 (June 1993).
	AP	2	Farrow, C.W., "A Continuously Variable Digital Delay Element," *ISCAS' 88*, IEEE, pp. 2641-2645 (1988).

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	AK	3	Fitz, M.P. and Lindsey, W.C., "Decision-Directed Burst-Mode Carrier Synchronization Techniques," *IEEE Transactions on Communications*, Vol. 40, No. 10, pp. 1644-1653 (October 1992).
	AL	3	Fowler, D.L. and Smith, J.E., "An Accurate, High Speed Implementation of Division by Reciprocal Approximation," *Proc. 9th Symp. On Computer Arithemtic*, pp. 60-67 (1989).
	AM	3	Freeman, H., *Discrete-Time Systems: An Introduction to the Theory,* John Wiley & Sons, Inc., Library of Congress Catalog Card Number 65-14255, Entire Book submitted (1965).
	AN	3	Fu, D. and Willson Jr., A.N., "Interpolation In Timing Recovery Using A Trigonometric Polynomial And Its Implementation," *Globecom 1998 Comm. Theory Mini Conf. Record*, IEEE, pp. 173-178 (November 1998).
	AO	3	Gardner, F.M., "Interpolation in Digital Modems - Part I: Fundamentals," *IEEE Transactions on Communications*, Vol. 41, No. 3, pp. 501-507 (March 1993).
	AP	3	Gardner, S., "Burst modem design techniques: part 1," *Electronic Engineering,* p. 85(5), (September 1999).

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	AK	4	Gardner, S., "Burst modem design techniques: part 2," *Electronic Engineering*, p. 75(5), (December1999).
	AL	4	Koren, I., *Computer Arithmetic Algorithms*, Prentice Hall, ISBN No. 0-13-151952-2, Entire book submitted (1993).
	AM	4	Lang, T. and Antelo, E., "CORDIC Vectoring with Arbitrary Target Value," *IEEE Transactions On Computers*, Vol. 47, No. 7, pp. 736-749 (July 1998).
	AN	4	Madisetti, A. *et al.*, "A 100-MHz, 16-b, Direct Digital Frequency Synthesizer with a 100-dBc Spurious-Free Dynamic Range," *IEEE Journal of Solid-State Circuits*, Vol. 34, No. 8, pp. 1034-1043 (August 1999).
	AO	4	Madisetti, A., *VLSI Architectures and IC Implementations for Bandwidth Efficient Communications*, Dissertation submitted to the University of California, Los Angeles, 132 pages (1996).
	AP	4	Meyr, H. *et al.*, *Digital Communication Receivers: Synchronization, Channel Estimation, and Signal Processing*, John Wiley & Sons, Inc., ISBN No. 0-471-50275-8, Entire book submitted (1998).

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	AA5						
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EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
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	AK	5	Moeneclaey, M., "A Simple Lower Bound on the Linearized Performance of Practical Symbol Synchronizers," *IEEE Transaction on Communications*, Vol. COM-31, No. 9, pp. 1029-1032 (September 1983).
	AL	5	Oerder, M. and Meyr, H., "Digital Filter and Square Timing Recovery," *IEEE Transactions on Communications*, Vol. 36, No. 5, pp. 605-612 (May 1988).
	AM	5	Pollet, T. and Peeters, M., "Synchronization with DMT Modulation," *IEEE Communications Magazine*, pp. 80-86 (April 1999).
	AN	5	Proakis, J. G., *Digital Communications, Third Edition*, McGraw-Hill, Inc., ISBN No. 0-07-051726-6, Entire book submitted (1995).
	AO	5	Proakis, J.G. and Manolakis, D.G., *Digital Signal Processing: Principles, Algorithms, and Applications, Second Edition*, Macmillan Publishing Company, ISBN No. 0-02-396815-X, Entire book submitted (1992).
	AP	5	Reimers, U., "Digital Video Broadcasting," *IEEE Communications Magazine*, pp. 104-110 (June 1998).

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	AA6						
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	AH6						
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	AK	6	Sabel, L.P. and Cowley, W.G., "A Recursive Algorithm For The Estimation Of Symbol Timing In PSK Burst Modems," *Proc. Globecom 1992*, Vol. 1, pp. 360-364 (1992).
	AL	6	Tan, L.K., *High Performance Architectures And Circuits For QAM Transceivers*, Dissertation submitted to the University of California, Los Angeles, 208 pages (1995).
	AM	6	Tan, L.K. and Samueli, H., "A 200 MHz Quadrature Digital Synthesizer/Mixer in 0.8μm CMOS," *IEEE Journal of Solid-State Circuits*, Vol. 30, No. 3, pp. 193-200 (March 1995).
	AN	6	Vankka, J., "Methods of Mapping from Phase to Sine Amplitude in Direct Digital Synthesis," *IEEE Transactions on Ultrasonics, Ferroelectrics, and Frequency Control*, Vol. 44, No. 2, pp. 526-534 (March 1997).
	AO	6	Vesma, J. and Saramäki, T., "Interpolation Filters With Arbitrary Frequency Response For All-Digital Receivers," *Proc. 1996 IEEE Int. Symp. Circuits Syst.*, pp. 568-571 (May 1996).
	AP	6	Vuori, J., "A Digital Multistandard Paging Receiver," *IEEE Transactions on Consumer Electronics*, Vol. 45, No. 4, pp. 1098-1103 (November 1999).

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	AA7						
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EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
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	AK	7	Wang, S. *et al.*, "Hybrid CORDIC Algorithms," *IEEE Transactions on Computers*, Vol. 46, No. 11, pp. 1202-1207 (November 1997).
	AL	7	Antelo, E. *et al.*, "Redundant CORDIC Rotator Based on Parallel Prediction," pp. 172, 179, IEEE (1995).
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